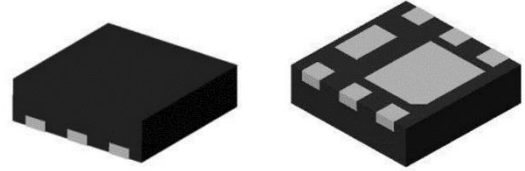


WNM3602A

SingleN-Channel, 30V,20.8A,Power MOSFET

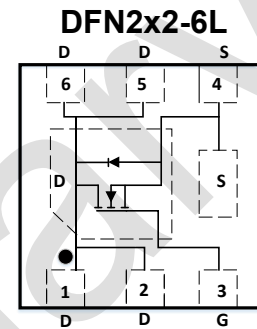
[http://www. omnivision-group.com](http://www.omnivision-group.com)

V _{DS} (V)	Max. R _{DS(on)} (mΩ)
30	4.7 @V _{GS} =10V
	7.3 @V _{GS} =4.5V



Description

The WNM3602A is N-Channel enhancement MOS Field Effect Transistor. This N-Channel MOSFET is produced using advanced Split Gate Trench process that has been optimized for R_{dson}, switching performance and ruggedness.



Pin configuration (Top view)

Features

- Split Gate Trench Technology
- Supper high density cell design
- Excellent ON resistance
- Package DFN2x2-6L



3602 = Device Code

NA = Special Code

Y = Year

W = Week(A~Z)

Marking

Applications

- DC/DC converters
- Power supply converters circuit
- Power Switching for portable device

Order information

Device	Package	Shipping
WNM3602A	DFN2x2-6L	3000/Tape&Reel

Absolute Maximum ratings

Parameter	Symbol	Maximum	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^e	I_D	$T_A=25^{\circ}C$	20.8
		$T_A=70^{\circ}C$	16.7
Pulsed Drain Current ^c	I_{DM}	106	A
Avalanche Energy $L=0.3mH$	E_{AS}	40.8	mJ
Power Dissipation ^a	P_D	$T_A=25^{\circ}C$	3.6
		$T_A=70^{\circ}C$	2.3
Operating Junction Temperature	T_J	-55 to 150	$^{\circ}C$
Storage Temperature Range	T_{STG}	-55 to 150	$^{\circ}C$

Thermal resistance ratings

Single Operation				
Parameter	Symbol	Maximum	Unit	
Junction-to-Ambient Thermal Resistance ^a	$R_{\theta JA}$	$t \leq 10 s$	35	$^{\circ}C/W$
		Steady State	67	
Junction-to-Ambient Thermal Resistance ^b	$R_{\theta JA}$	$t \leq 10 s$	132	
		Steady State	209	

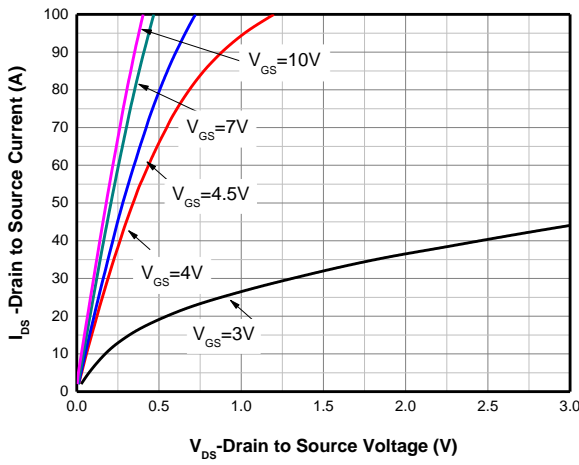
Note:

- a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm² area)
- b FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) minimum pad covered with copper
- c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial $T_J = 25^{\circ}C$, the maximum allowed junction temperature of $150^{\circ}C$.
- d The static characteristics are obtained using ~380us pulses, duty cycle ~1%.
- e The power dissipation P_D is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ $t \leq 10s$ value and the $T_{J(MAX)} = 150^{\circ}C$.

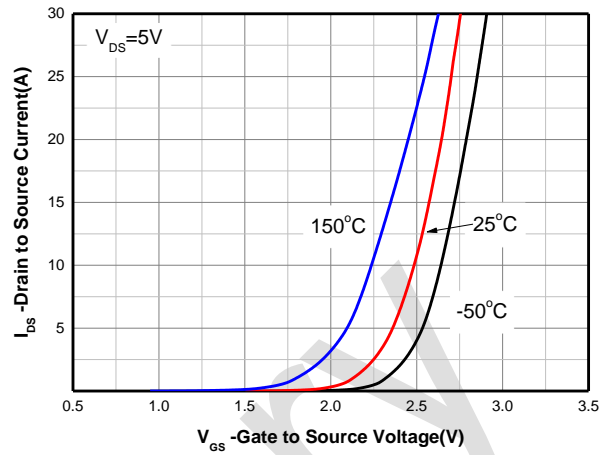
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 250\mu\text{A}$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	μA
Gate-to-source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.2	1.6	2.2	V
Drain-to-source On-resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 18\text{ A}$		3.7	4.7	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 18\text{ A}$		5.4	7.3	
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz},$ $V_{DS} = 15\text{ V}$		854.0		pF
Output Capacitance	C_{OSS}			550.4		
Reverse Transfer Capacitance	C_{RSS}			17.8		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 18\text{ A}$		16.2		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 18\text{ A}$		7.8		
Gate-to-Source Charge	Q_{GS}	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 18\text{ A}$		3.3		
Gate-to-Drain Charge	Q_{GD}	$I_D = 18\text{ A}$		1.9		
Gate Resistance	R_g	$f = 1\text{ MHz}$		2.0		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_d(ON)$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 18\text{ A}, R_G = 3\Omega$		5.1		ns
Rise Time	t_r			49.0		
Turn-Off Delay Time	$t_d(OFF)$			15.0		
Fall Time	t_f			3.8		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 1\text{ A}$		0.7	1.2	V
Reverse Recovery Time	t_{rr}	$I_F = 18\text{ A},$		24.8		nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{ A}/\mu\text{s}$		8.9		nC

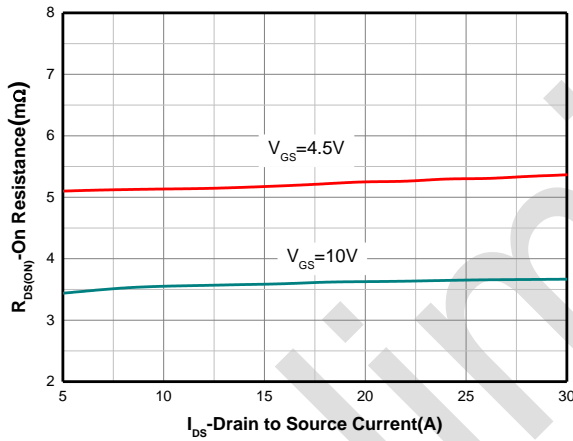
Typical Characteristics (Ta=25°C, unless otherwise noted)



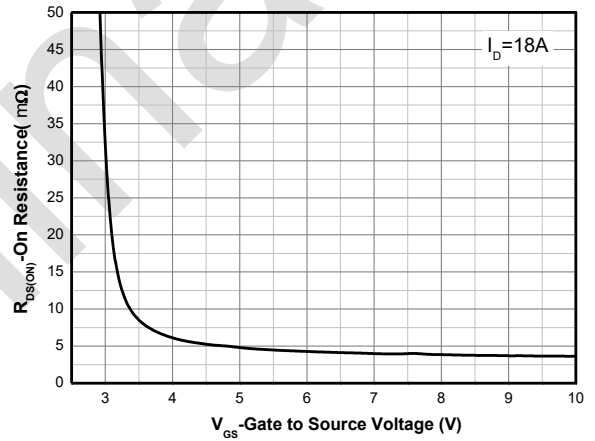
Output Characteristics ^d



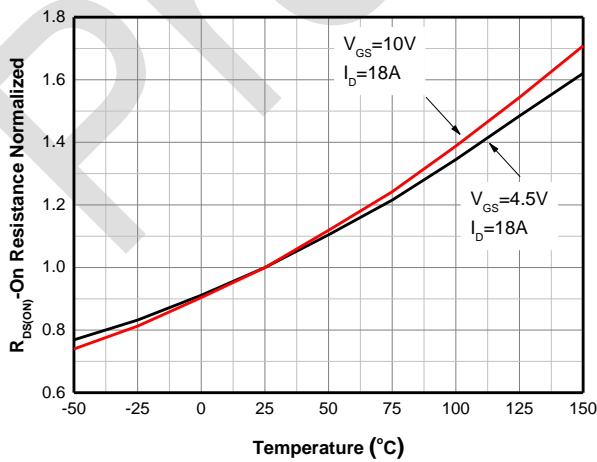
Transfer Characteristics ^d



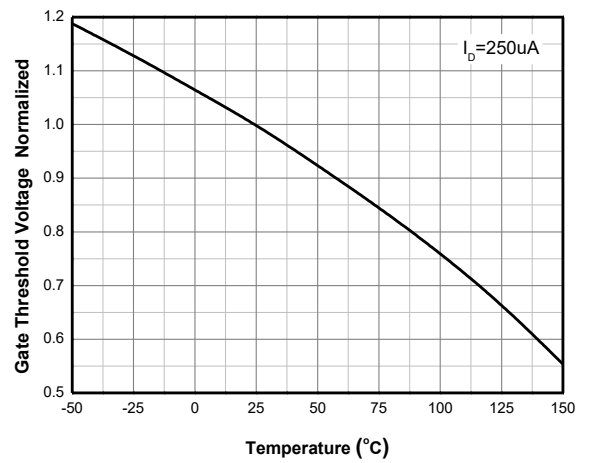
On-Resistance vs. Drain Current ^d



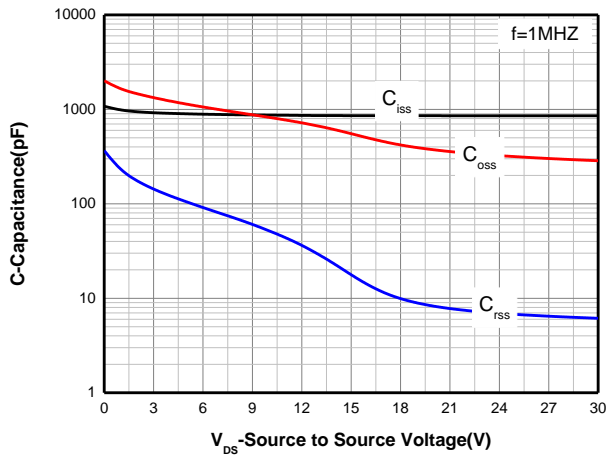
On-Resistance vs. V_{GS} ^d



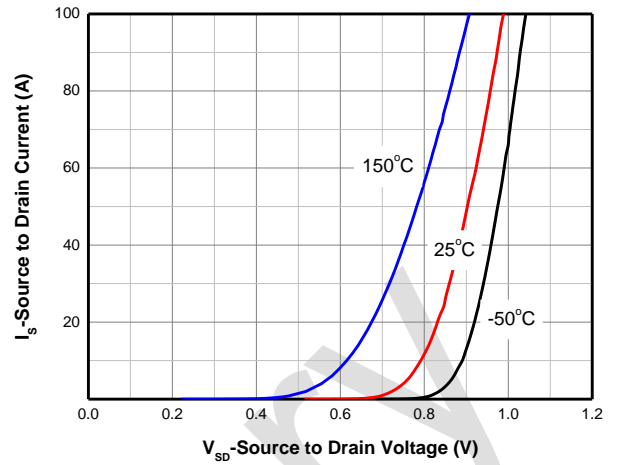
On-Resistance vs. Junction Temperature ^d



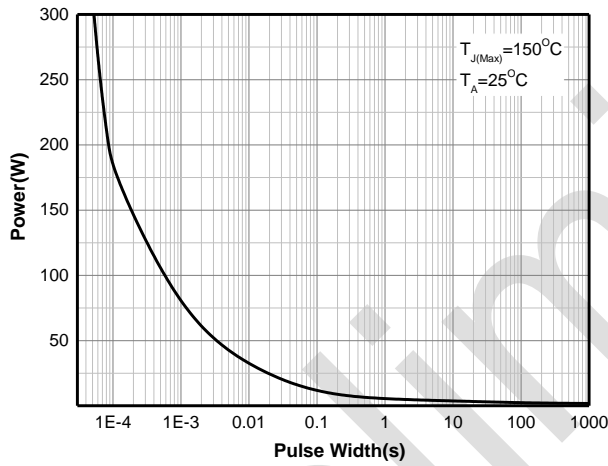
Threshold Voltage vs. Temperature



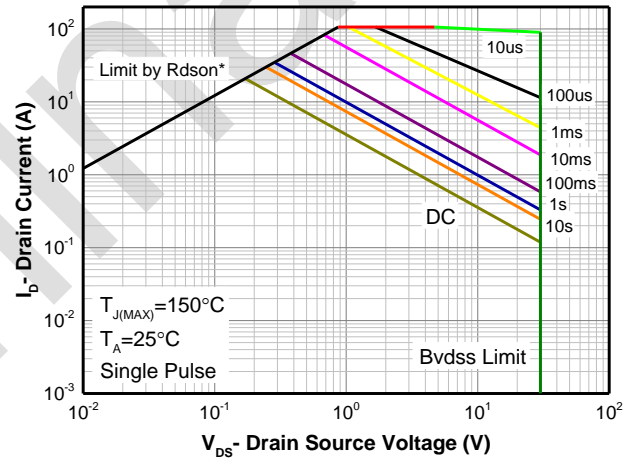
Capacitance



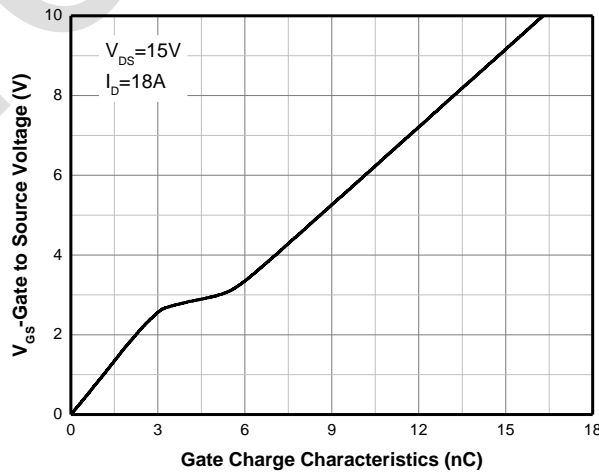
Body Diode Forward Voltage^d



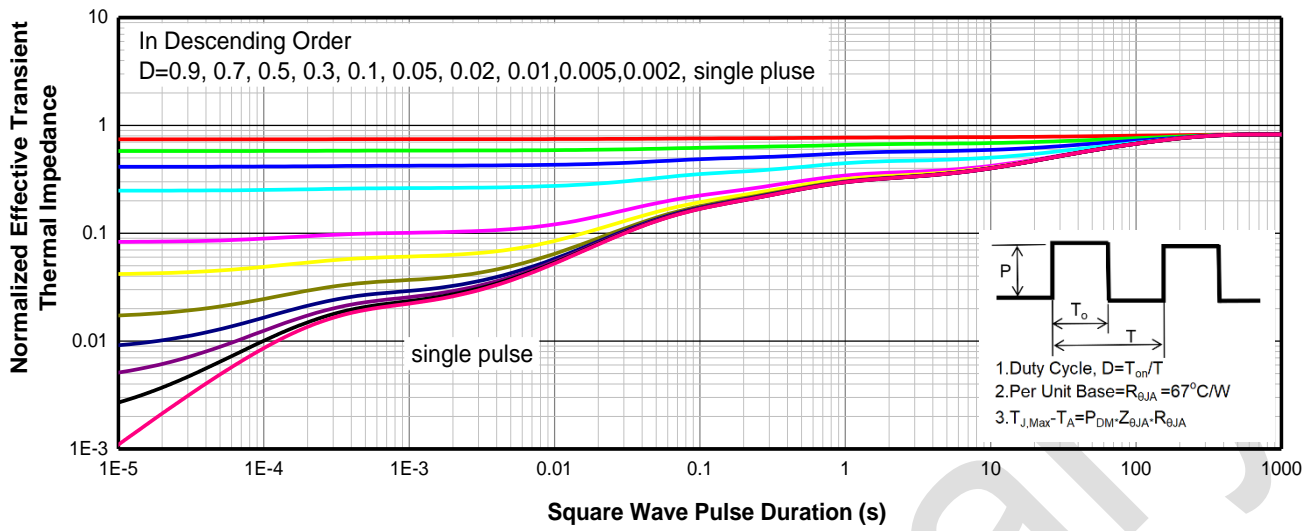
Single Pulse power



Safe Operating Area



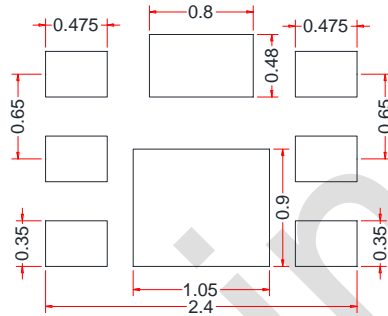
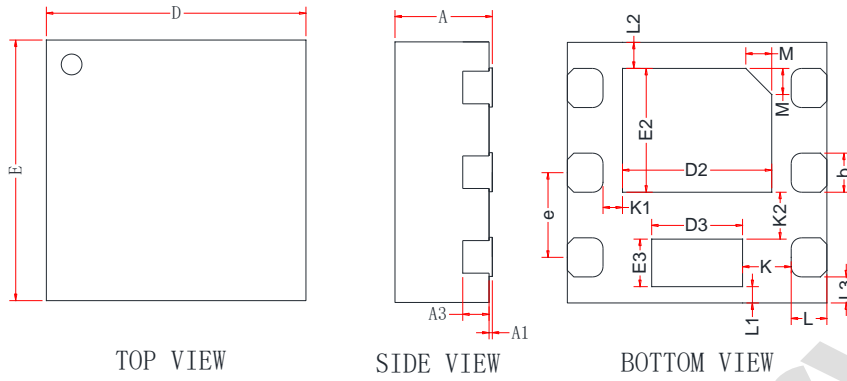
Gate Charge Characteristics



Transient Thermal Response (Junction-Ambient)

PACKAGE OUTLINE DIMENSIONS

DFN2x2-6L

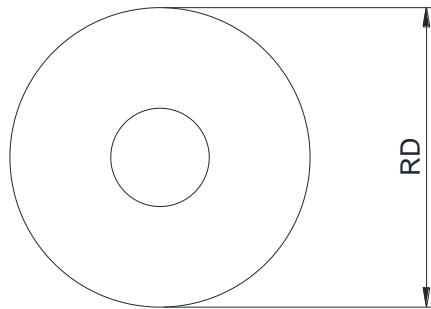


RECOMMENDED LAND PATTERN (Unit:mm)

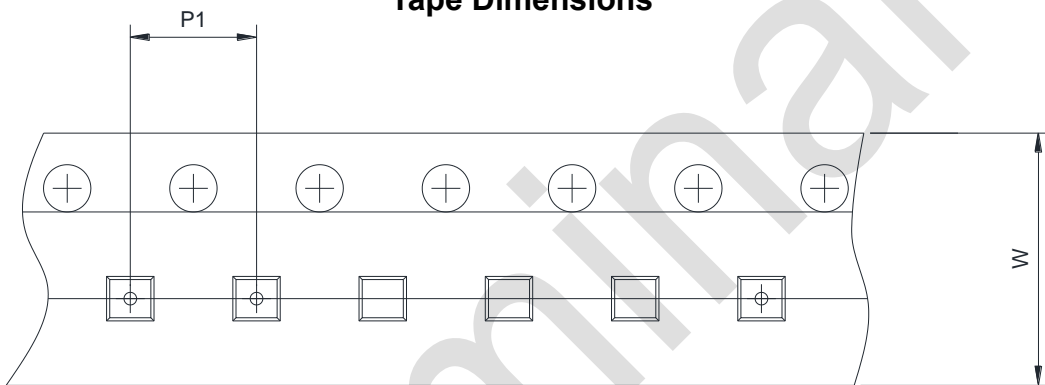
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 Ref.		
b	0.25	0.30	0.35
D	1.95	2.00	2.05
E	1.95	2.00	2.05
D2	1.05	1.15	1.25
E2	0.85	0.95	1.05
D3	0.60	0.70	0.80
E3	0.265	0.365	0.465
e	0.55	0.65	0.75
K	0.37 REF		
K1	0.15 REF		
K2	0.36 REF		
L	0.225	0.275	0.325
L1	0.125 REF		
L3	0.20 REF		
L3	0.20 REF		
M	0.20 REF		

TAPE AND REEL INFORMATION

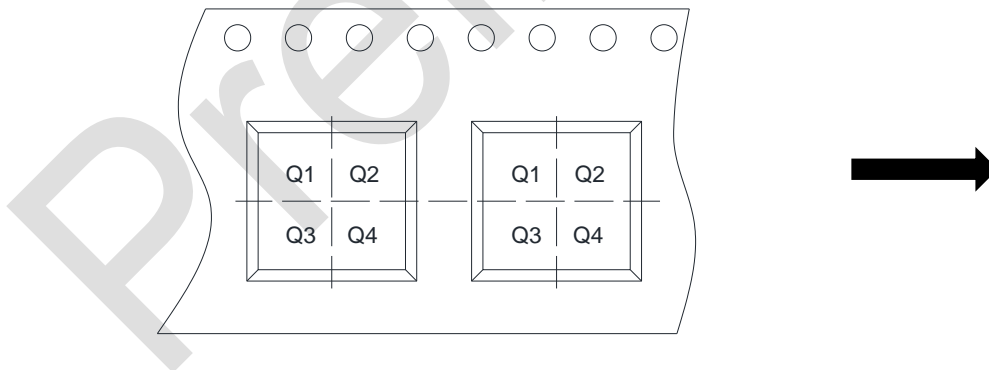
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	<input checked="" type="checkbox"/> 7inch	<input type="checkbox"/> 13inch
W	Overall width of the carrier tape	<input checked="" type="checkbox"/> 8mm	<input type="checkbox"/> 12mm <input type="checkbox"/> 16mm
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input checked="" type="checkbox"/> 4mm <input type="checkbox"/> 8mm
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2 <input type="checkbox"/> Q3 <input type="checkbox"/> Q4